Degradation of AlGaN/GaN HEMTs under DC and RF Stress

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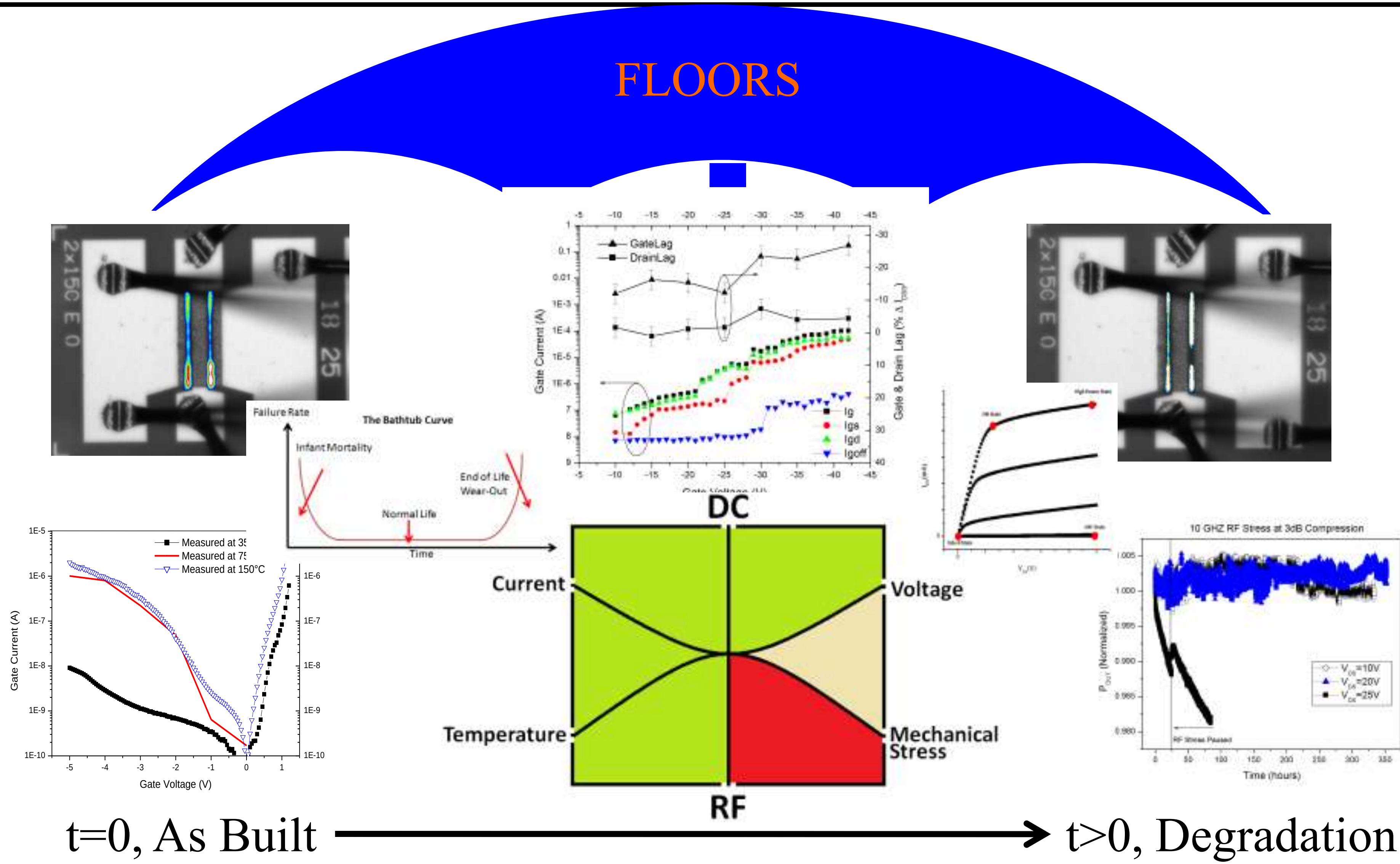
Electrical Characterization & Stress



Overview

I. Introduction

II. DC Stress Results

A. Off-State Stress – EL & PL

B. Temperature Dependent Off-State Stress

C. Gate and Drain Lag

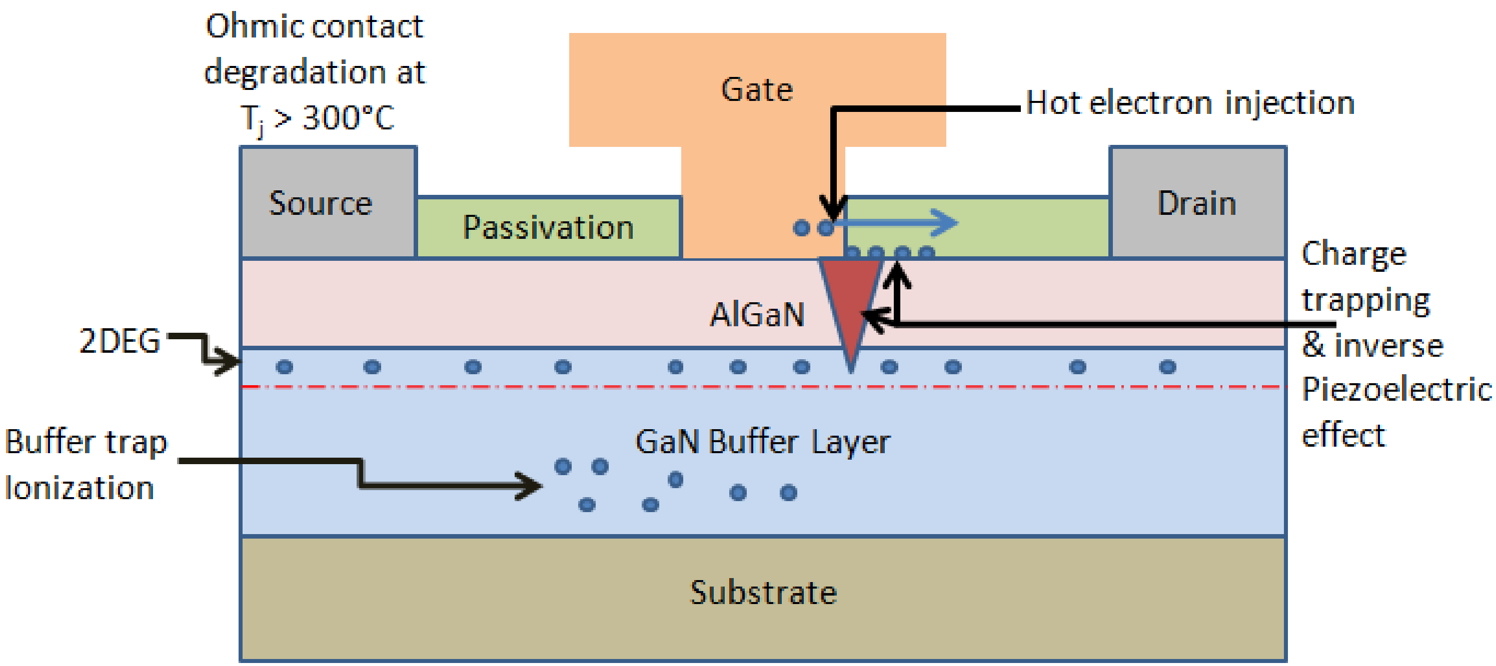
III. RF Stress Results

A. Drain Bias Dependence

B. Photoemission

IV. Conclusion

Introduction

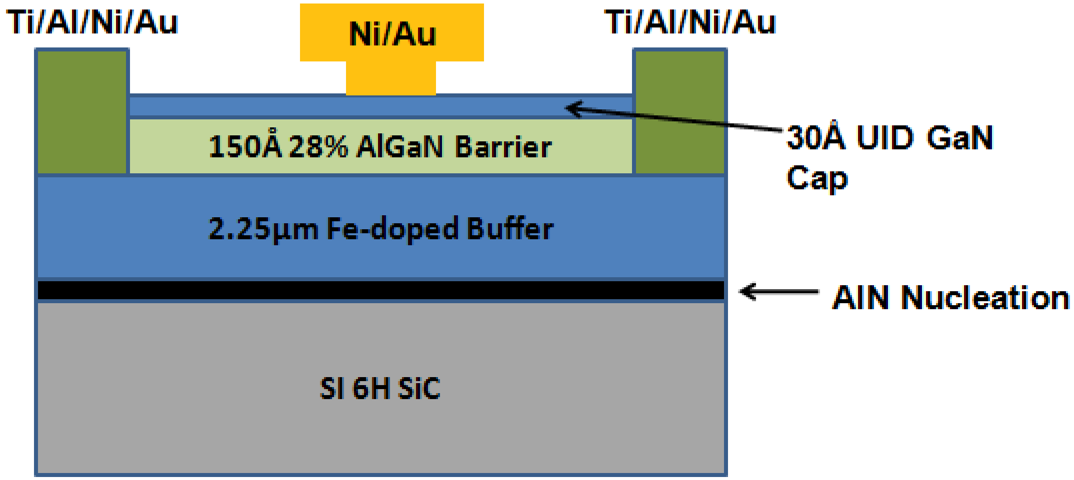


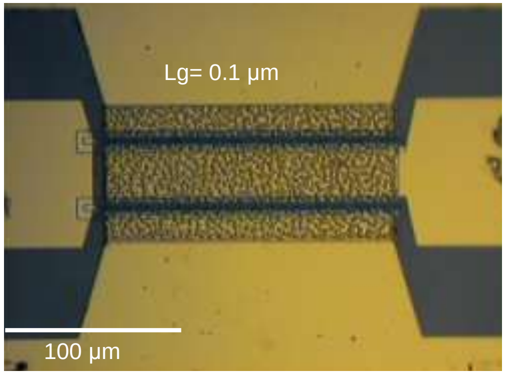
Degradation Mechanisms:

1) Hot Electrons
2) Contact Degradation
3) Inverse Piezoelectric Effect

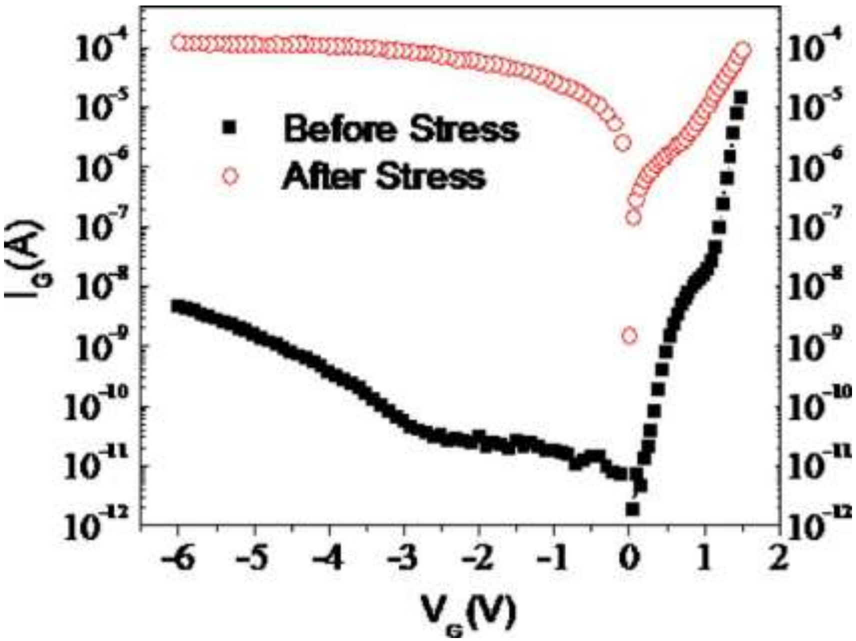
Stress Conditions (DC)

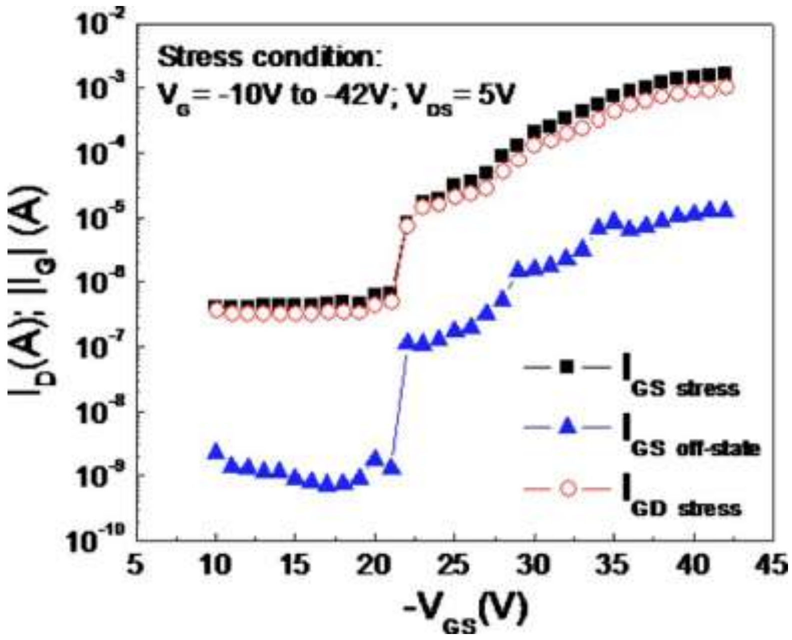
- AFRL AlGaN/GaN HEMTs with Ni/Au gate on SiC
- 0.14 µm gate step-stressed from -10 V to -42 V in -1 V step (V_{DS}= 0V).
- Temperature of device regulated by heated chuck (25 ° C– 150 ° C).





DC Off-State Stress

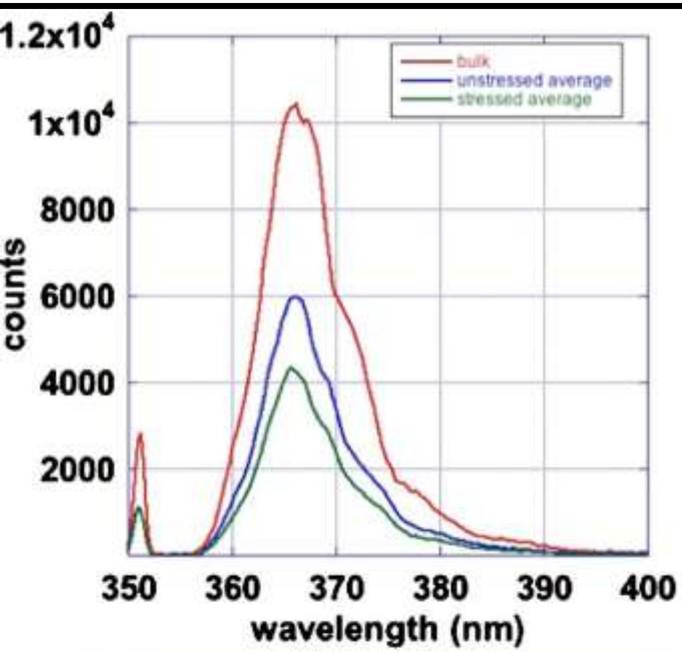


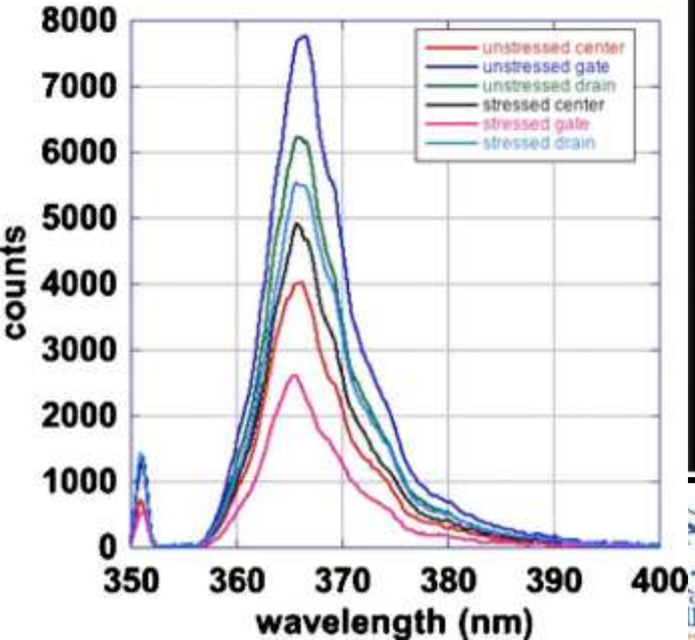


- HEMTs with 0.14 µm gate length step stressed from -10 V to -42 V at -1V/min. V_{DS} = 5V.
- V_{CRI} = -21 V

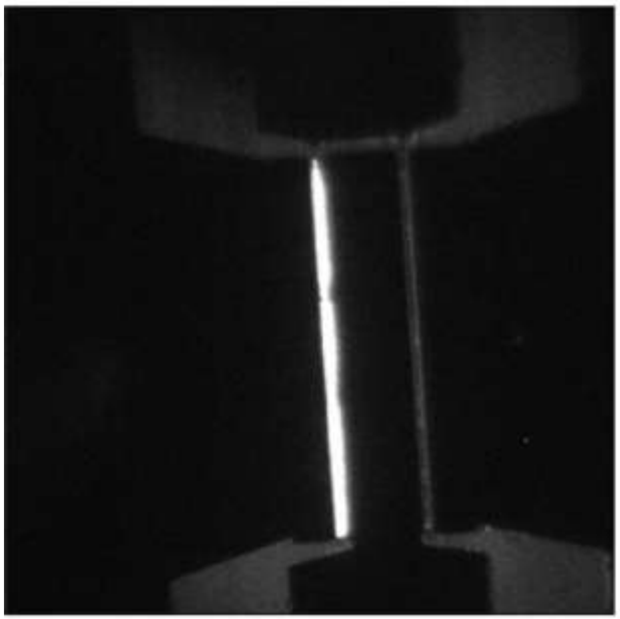
C.-Y. Chang, *et al.*, *Journal of Vacuum Science & Technology B,* vol. 28, pp. 1044-1047, 2010.

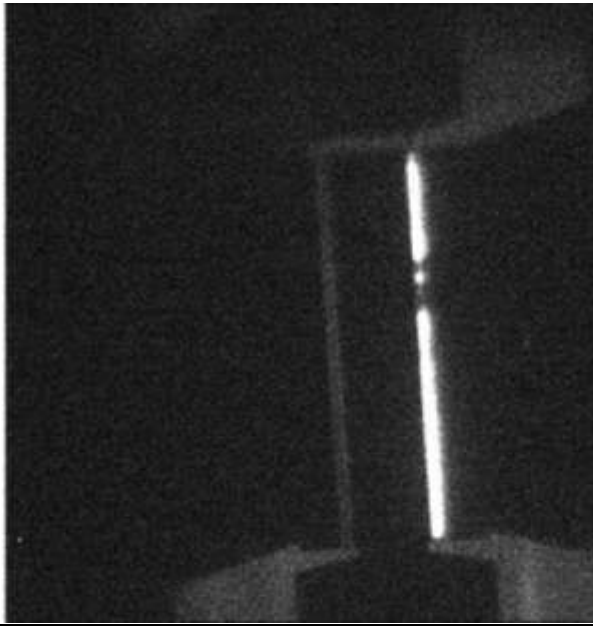
EL & PL





- PL shows non-radiative trap formation increases after stress.
- EL indicates failure may be localized along gate length.





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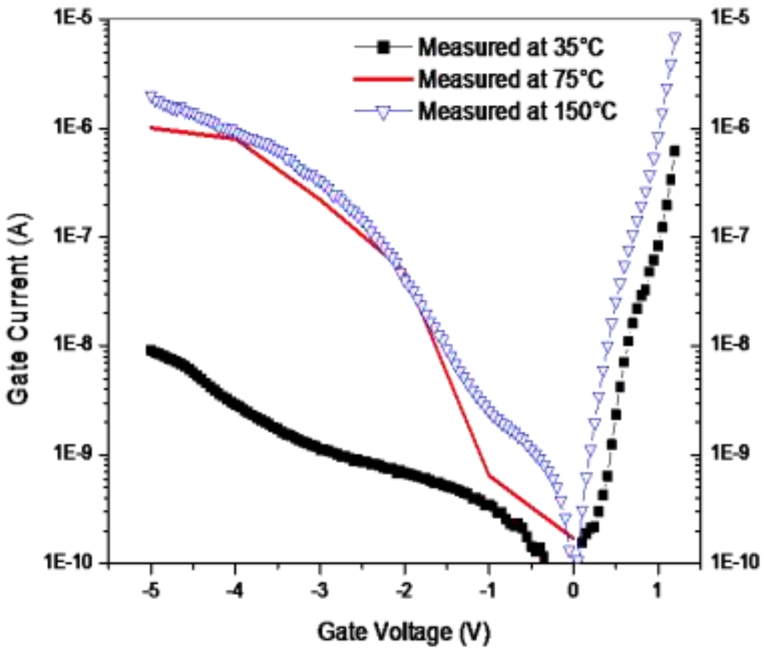
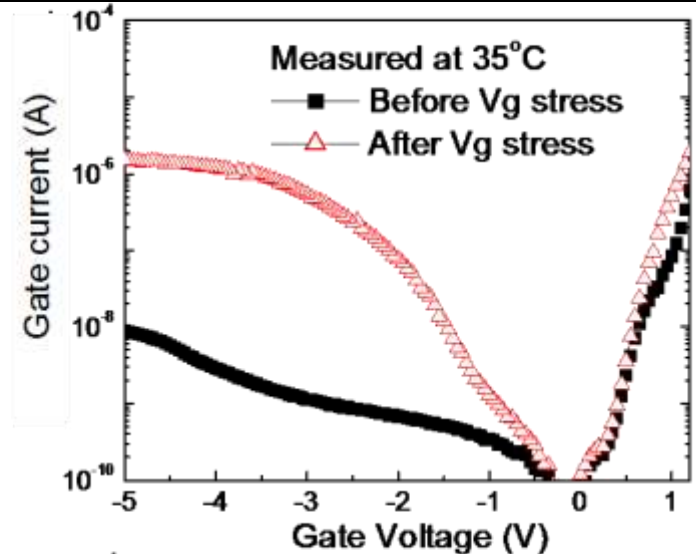
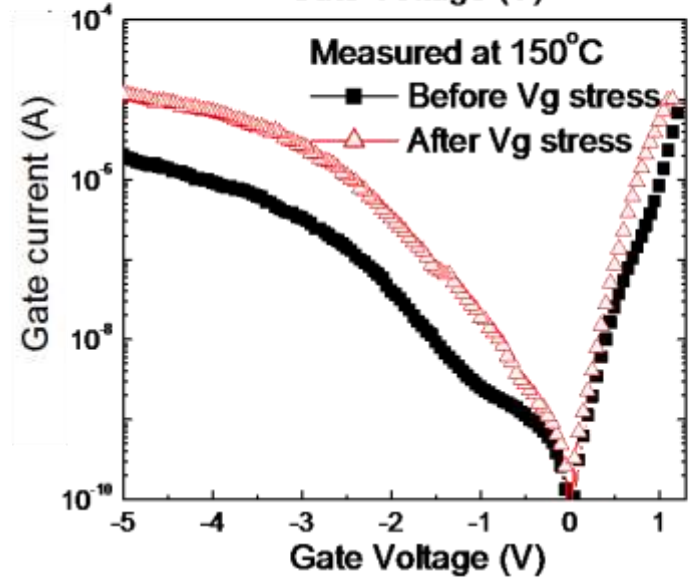
Temperature Dependence V_{CRI}

- Increase in leakage current with temperature.
- Total increase in leakage current decreases.

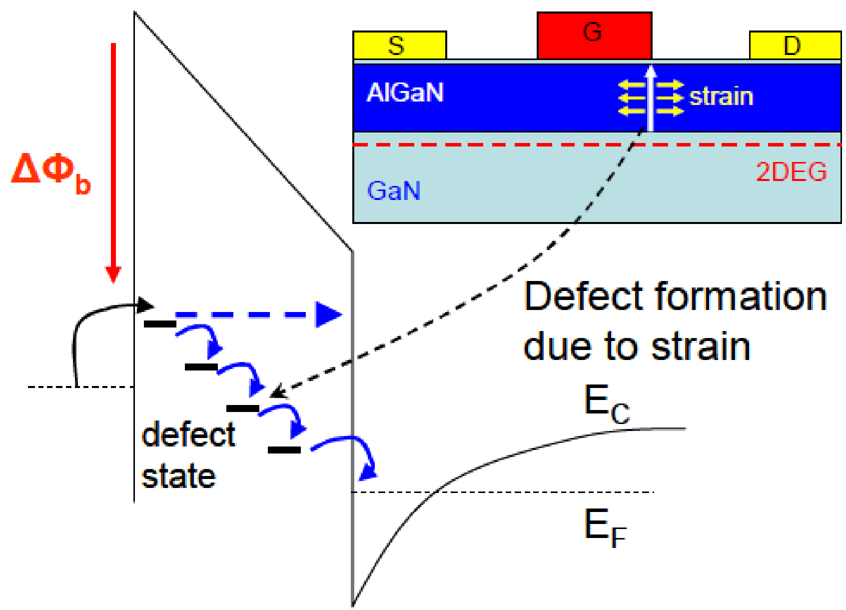


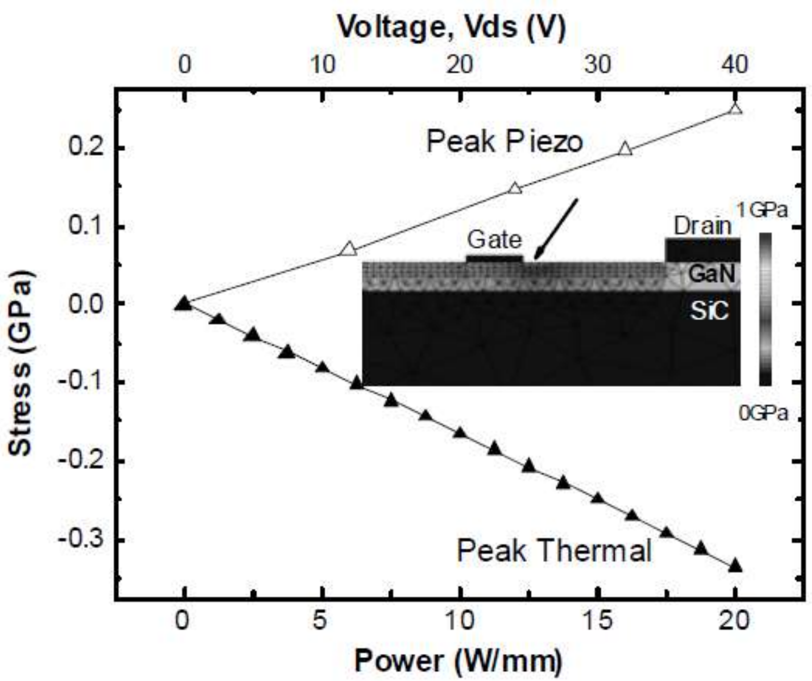




E. A. Douglas, *et al.*, *submitted to Microelectronics Reliability*

Temperature Dependence V_{CRI} (2)

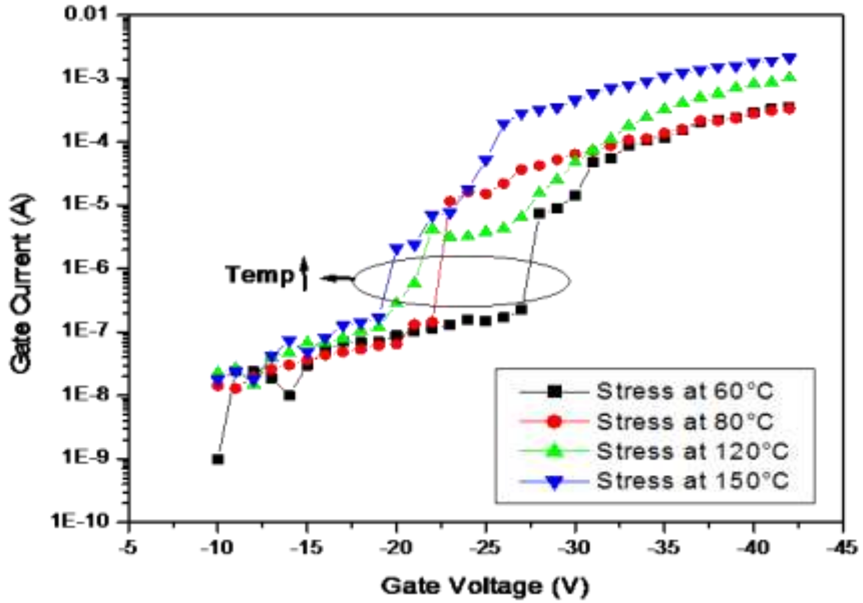


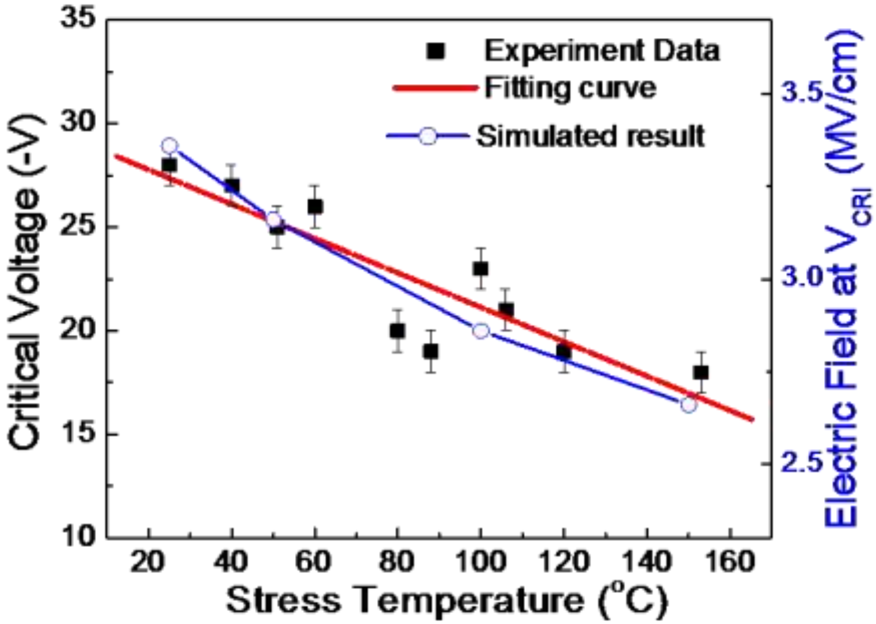


J. A. del Alamo, J. Joh. Microelectronics Reliability, 49 (2009) 1200–1206.

A. Sarua, et al. Proc. CS Mantech Conf. 8.5 (2009).

Temperature Dependence V_{CRI} (3)

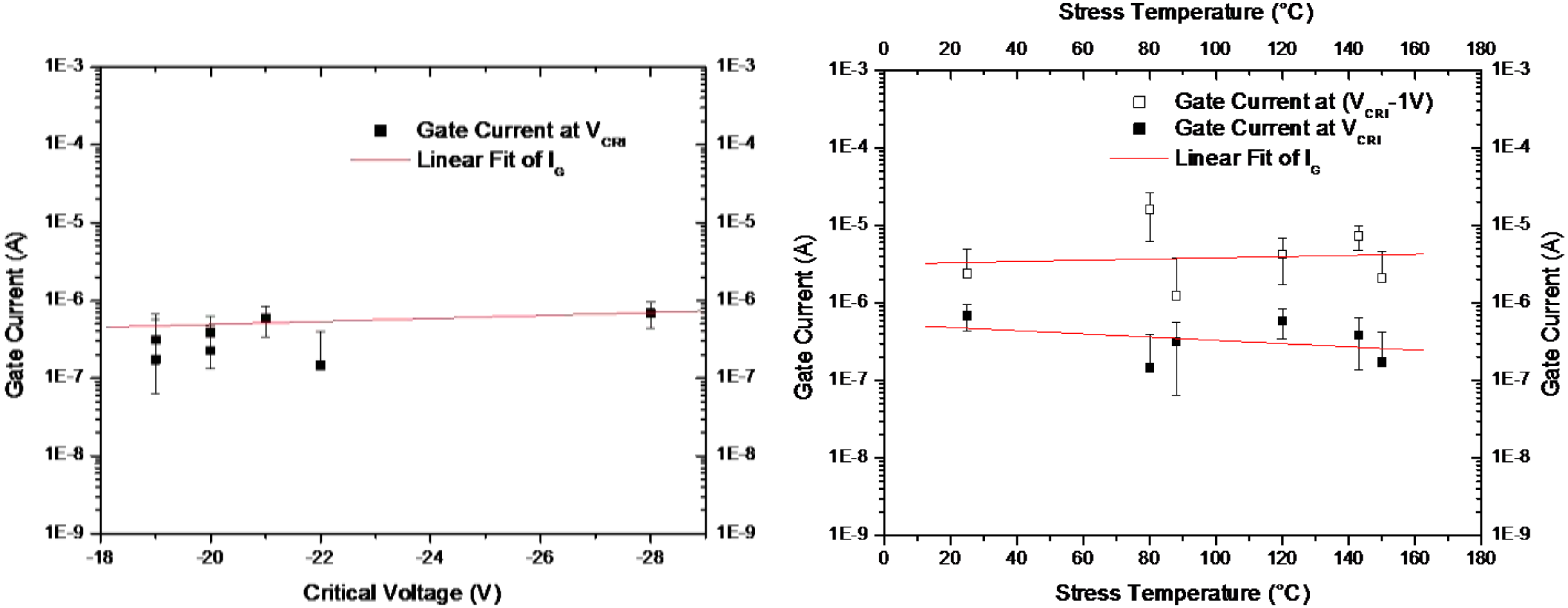




- Critical voltage decreases with increasing temperature.
- Linear dependence observed.

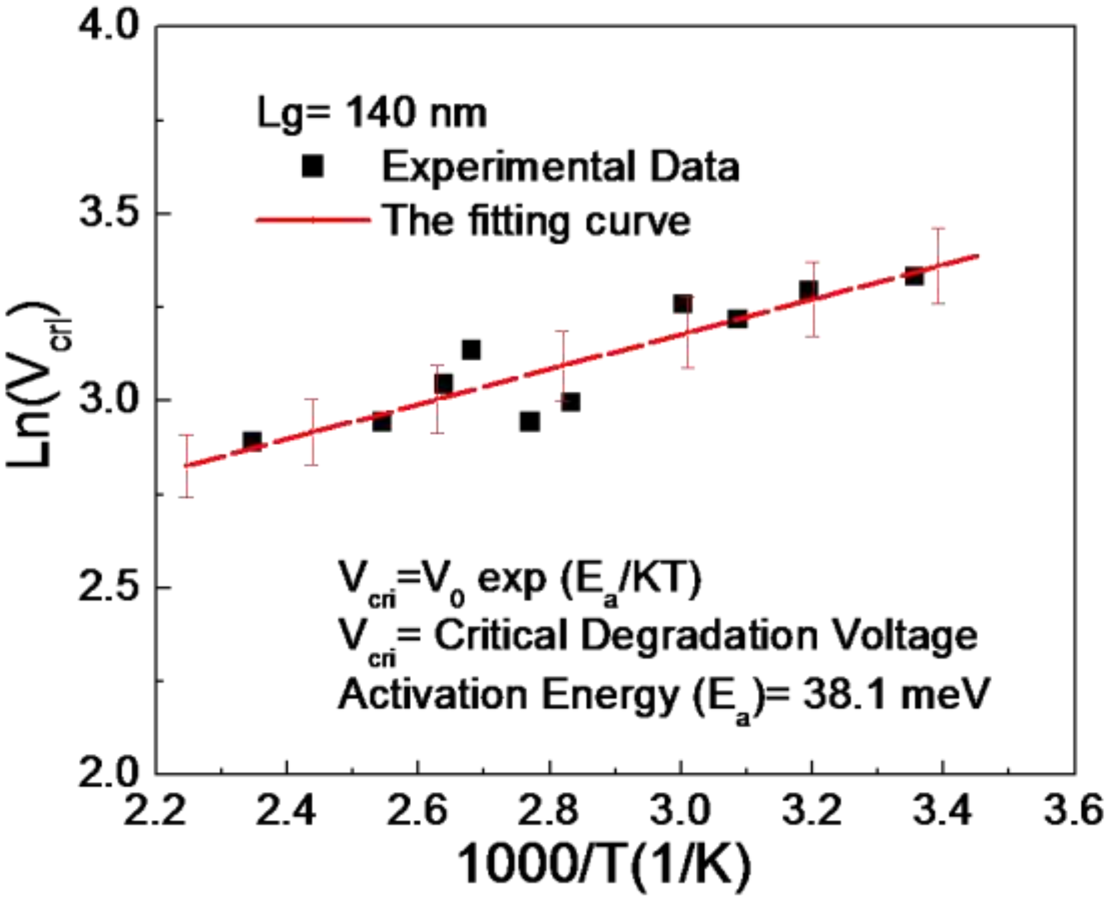
Temperature Dependence V_{CRI} (4)

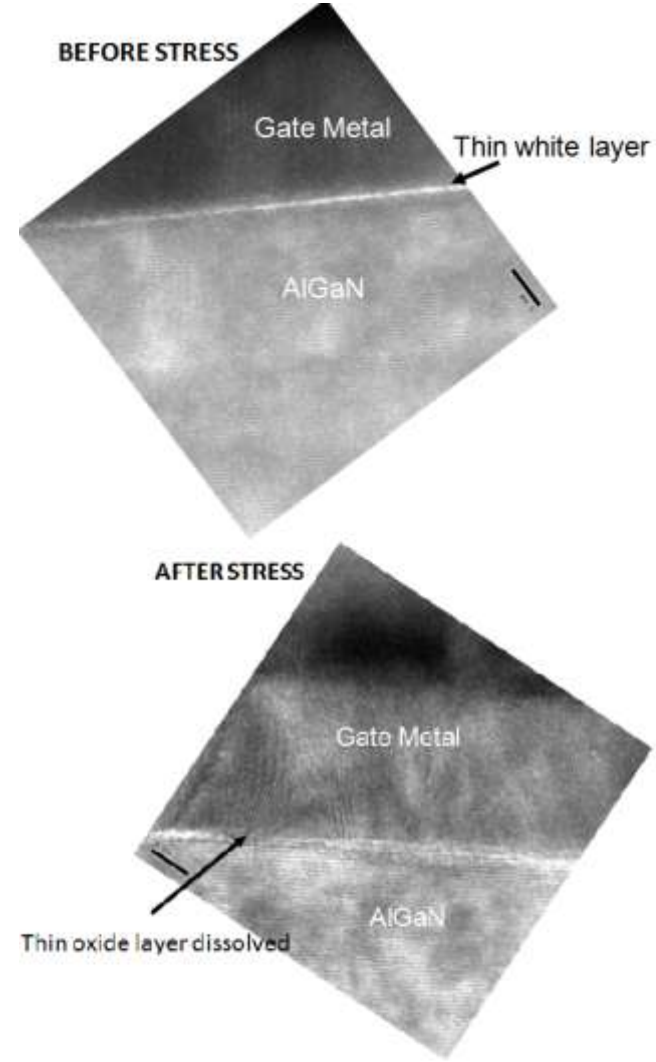
- Gate leakage current similar, independent of critical voltage.
- Current similar **at** and immediately **after** V_{CRI}



Temperature Dependence V_{CRI} (5)

- Small activation energy: 38.1 meV

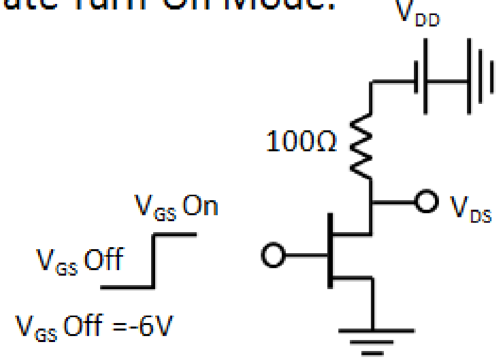




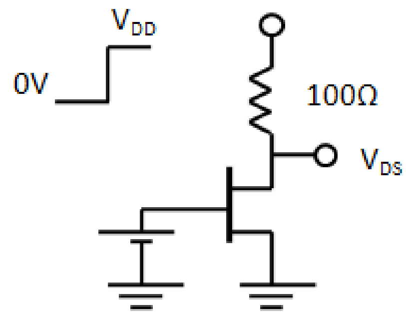
Overview

Gate & Drain Lag

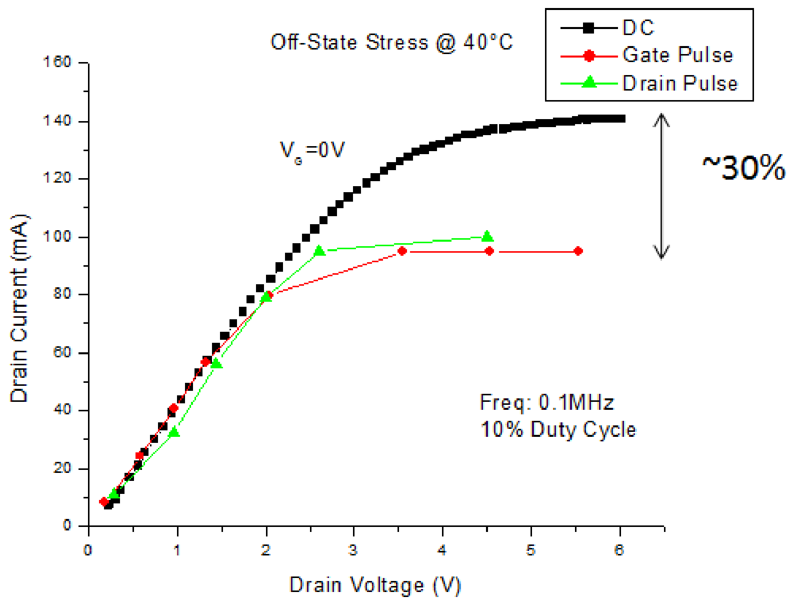
A) Gate Turn-On Mode:

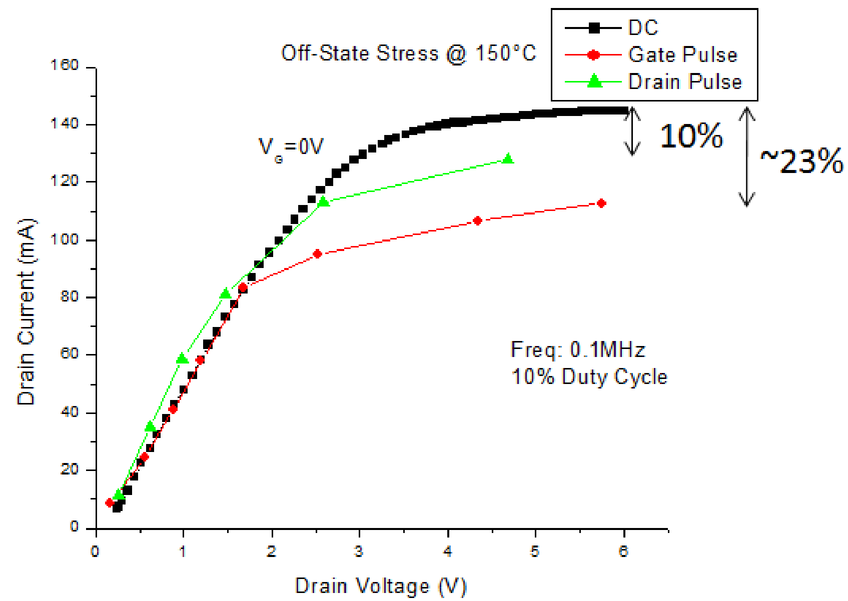


B) Drain Turn-On Mode:



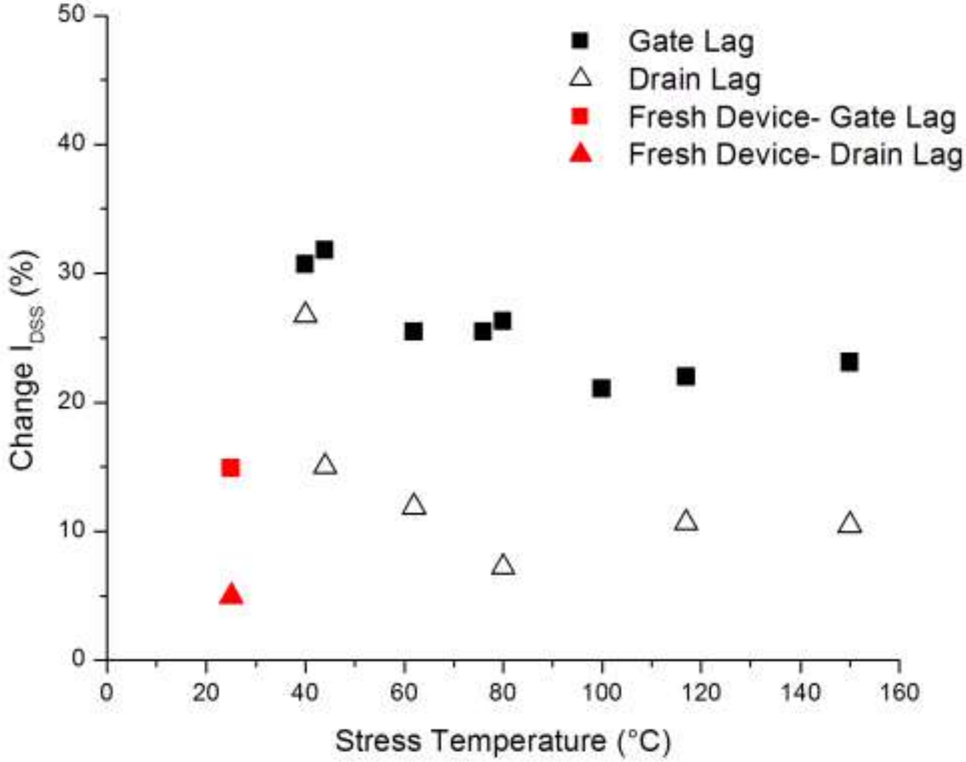
Gate and drain pulsed at 0.1 MHz, 10% duty cycle at room temperature



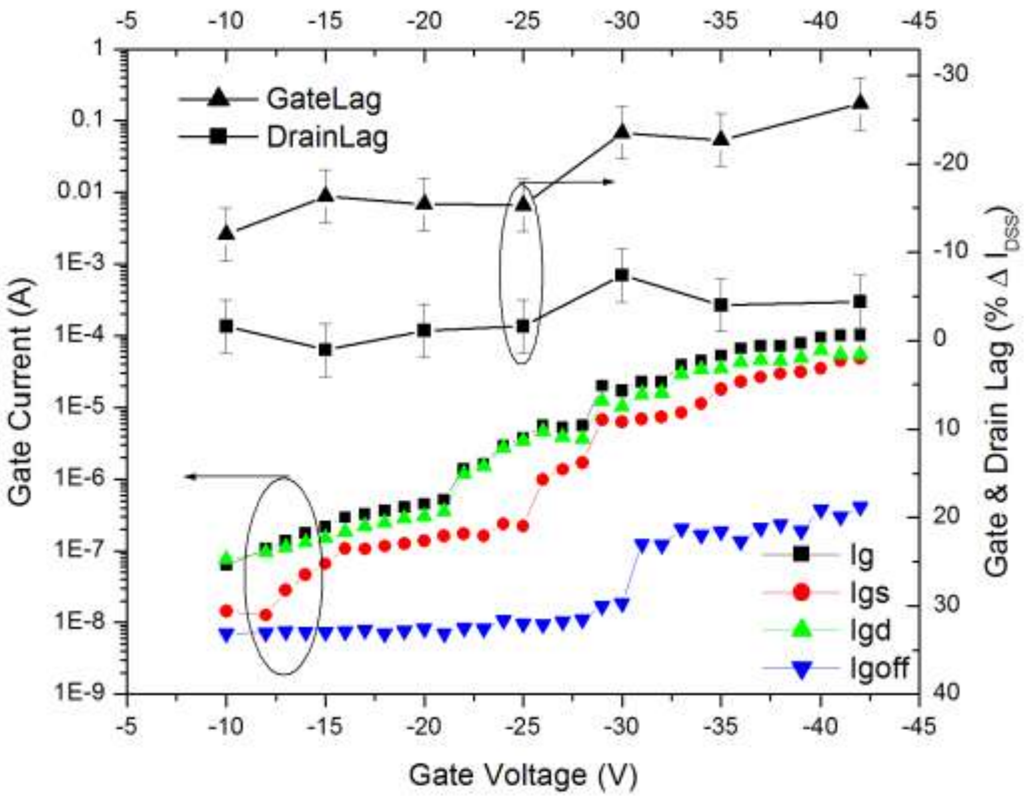


Gate & Drain Lag (2)

- Gate and drain lag increases substantially after stress.
- As stress temperature increases, gate and drain lag decreases (non-linear).
- Trap formation changes with stress temperature.



Gate & Drain Lag (3)



- Step-like increase in I_G observed after V_{CRI}
- Drain lag increases slowly
- Sharp rise in gate lag **after** second sharp step in I_G
- Shallow traps predominant after stressing

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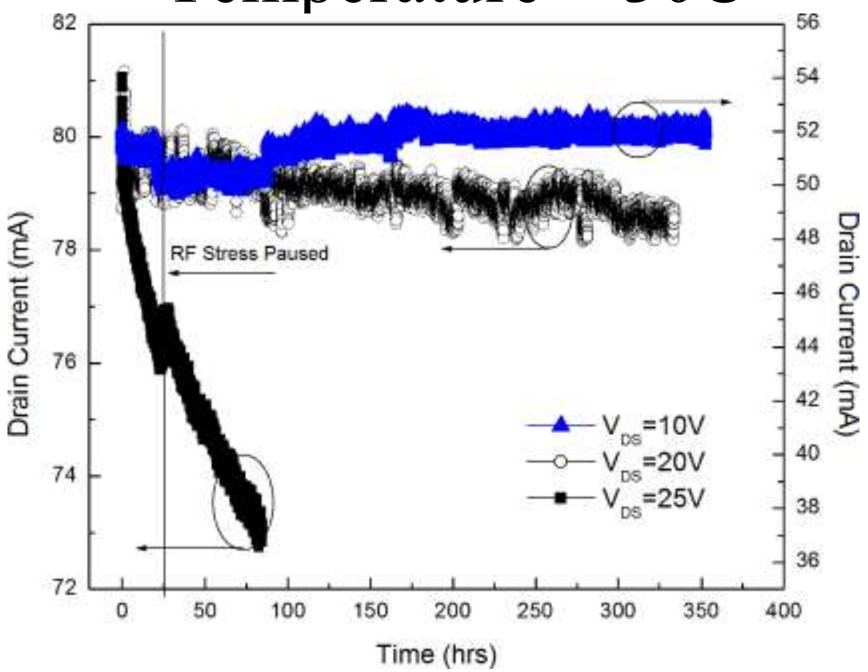
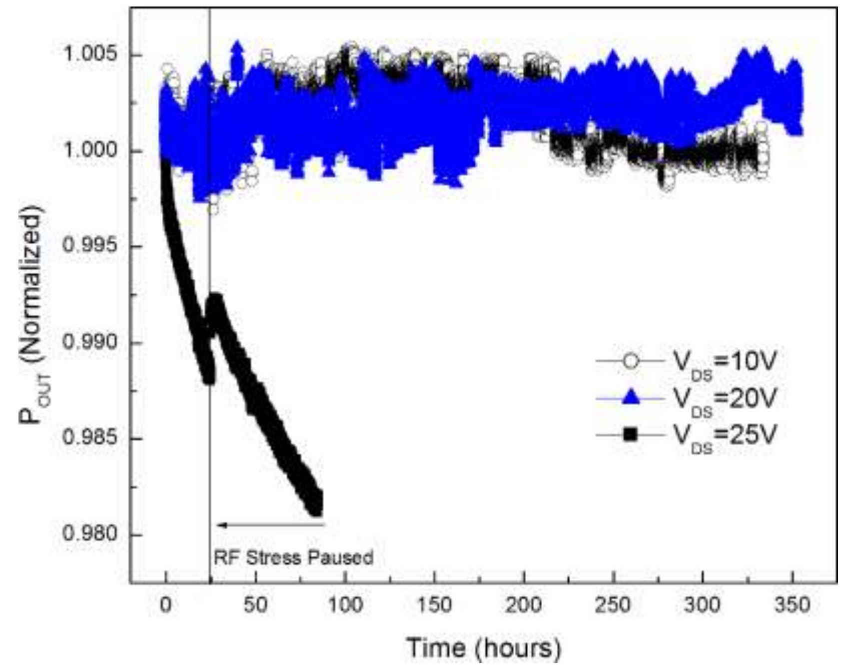
Stress Conditions (RF)

- Stressed at AFRL on AccelRF system
- 0.125 µm gate length, 10 GHz stress at 3 dB and 3.7 dB compression point
- Class AB condition, I_{DQ} = 200mA/mm
- Baseplate temperature from 30 – 120° C

RF Stress – Drain Bias

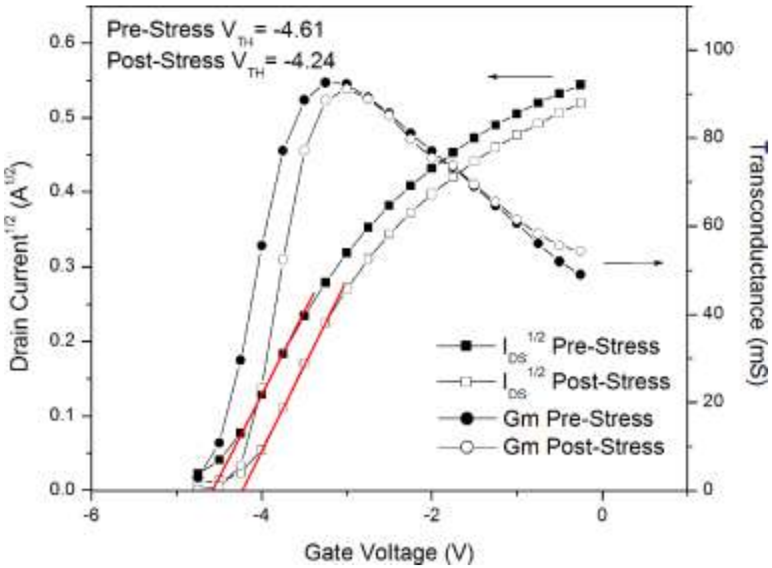
- Devices stressed at V_{DS} = 10, 20, 25, 30 V
- V_{DS} = 30 V resulted in catastrophic failure
- Up to 350 hours RF stress
- Temperature = 30C

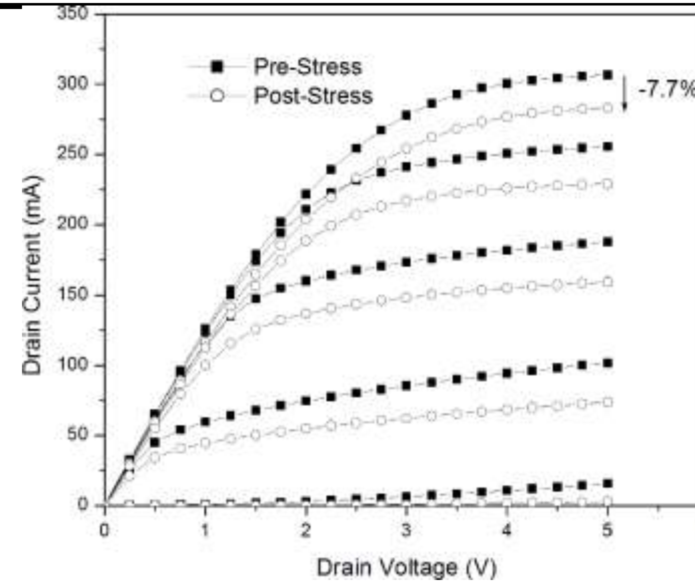




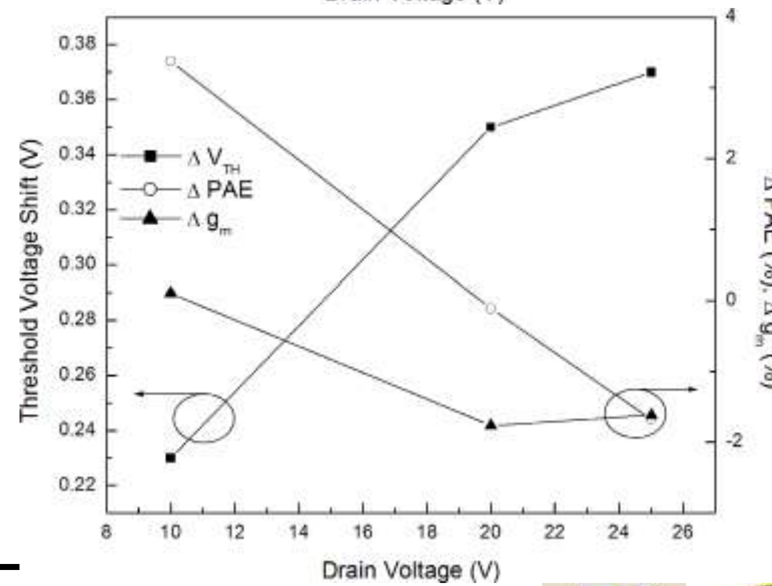
E. A. Douglas, *et al.*, *submitted to Applied Physics Letters*

RF Stress – Drain Bias (2)



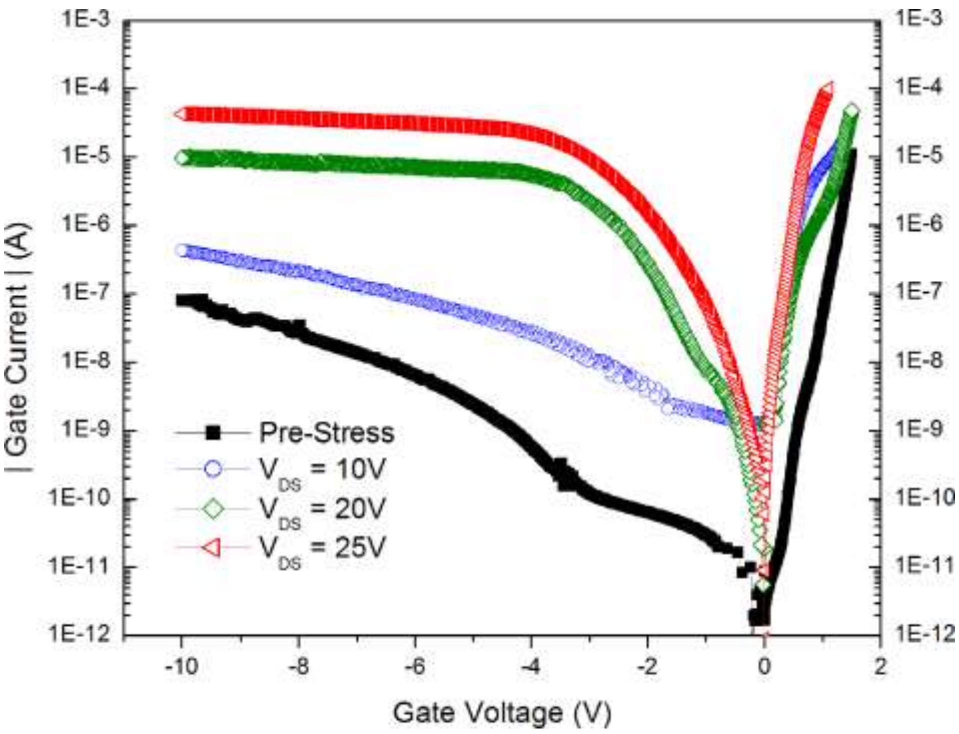


- I_{DSS}, g_m, PAE, and gain show minimal degradation.
- Large shifts in V_{TH}
- Dissipated power at 20V and 25V are 3.5 W/mm and 3.77 W/mm

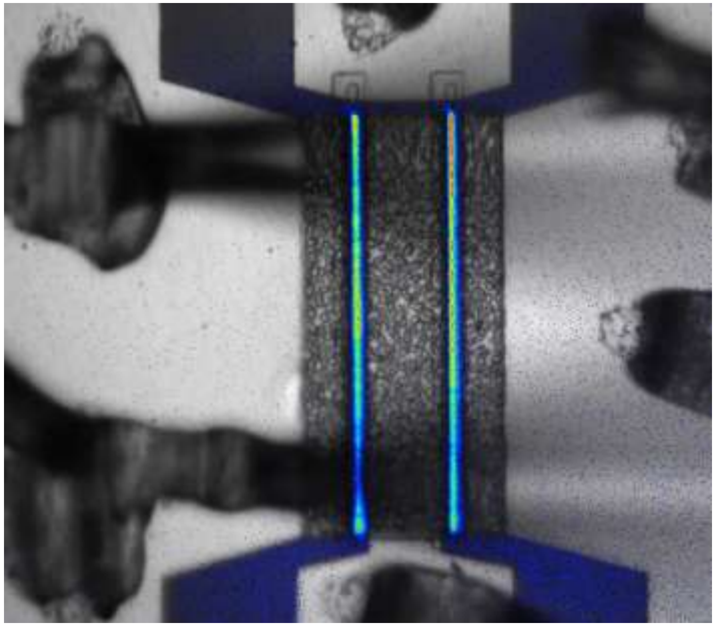
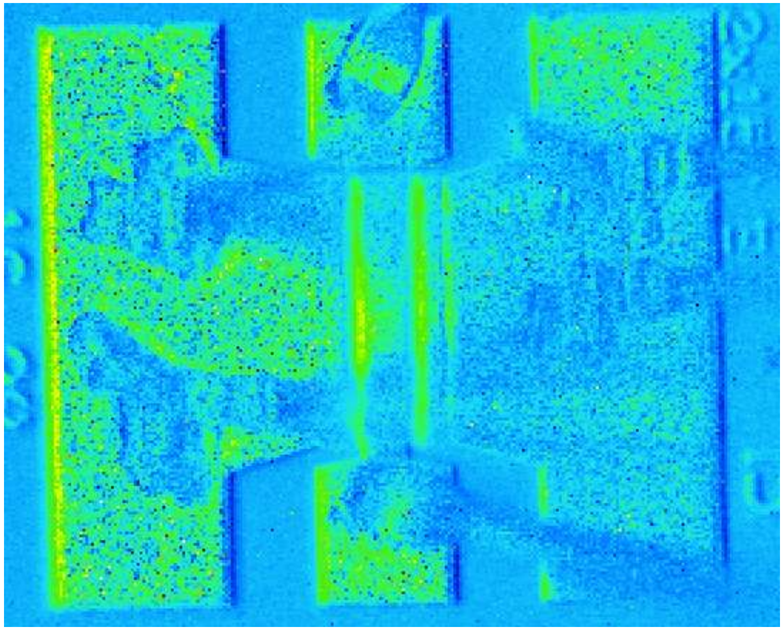


RF Stress – Drain Bias (3)

- Gate leakage current increases several orders of magnitude.
- Schottky barrier height decreases from 673 mV to 602 mV
- Schottky contact likely point of degradation
- $E_A = 0.45$ eV



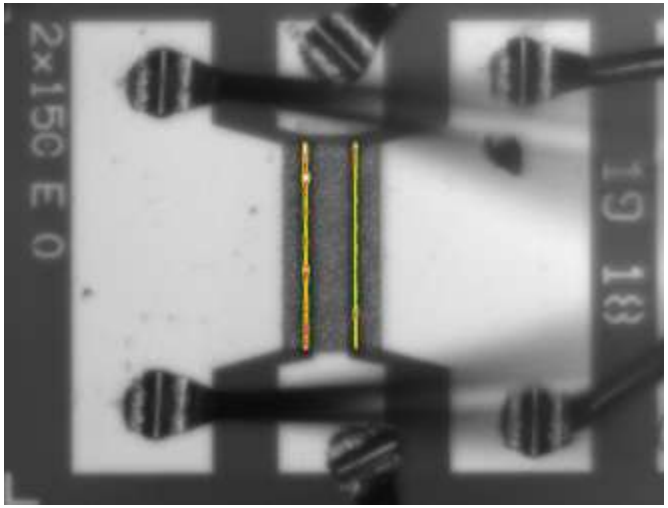
Photoemission

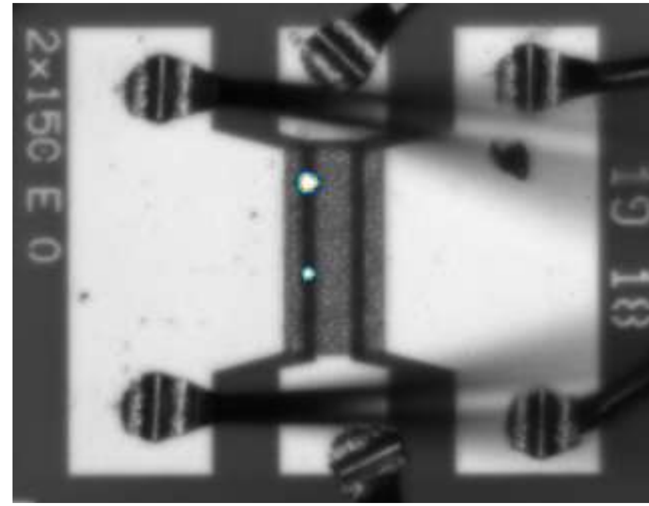
Photo emission	Thermal emission
	
I_{DS} ~ 30 mA	Max Temp ~75 C with baseplate at 70C

Photoemission (2)

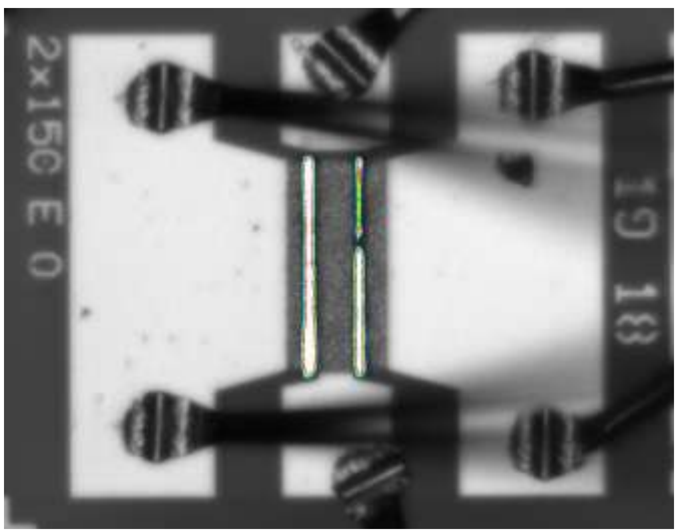
Forward Bias | Reverse Bias

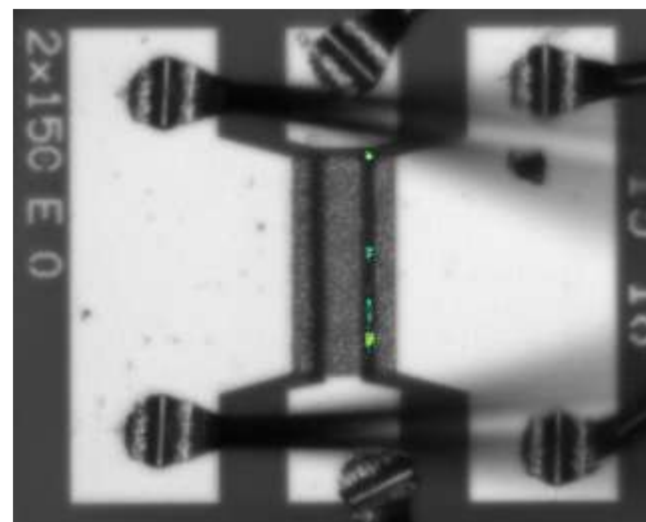
Pre-Stress





Post-Stress





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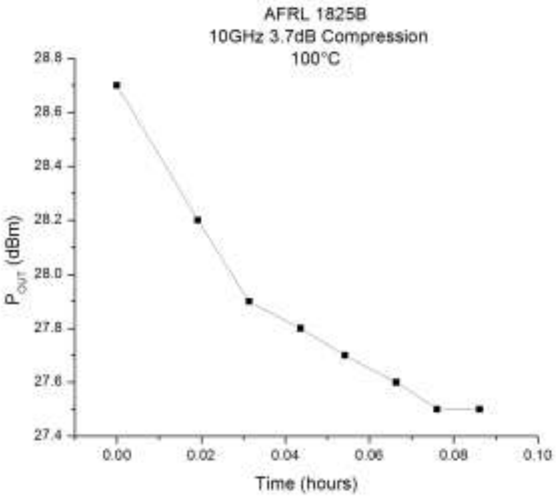
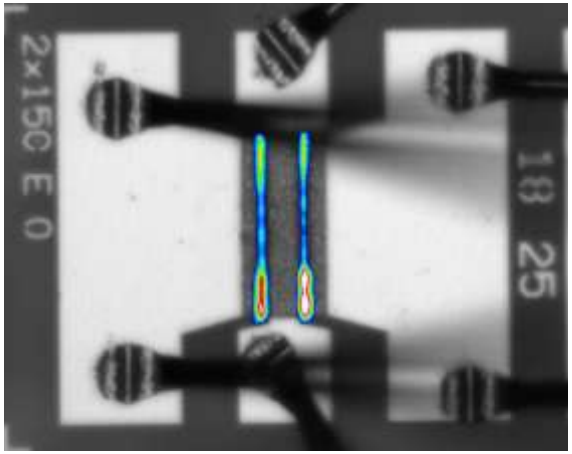
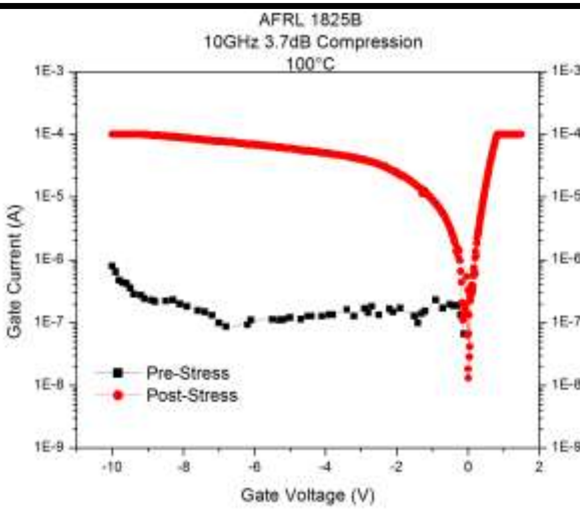
Photoemission (3)

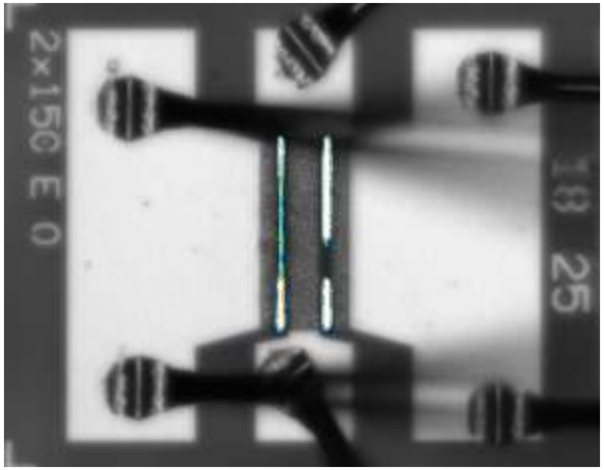


Forward Bias

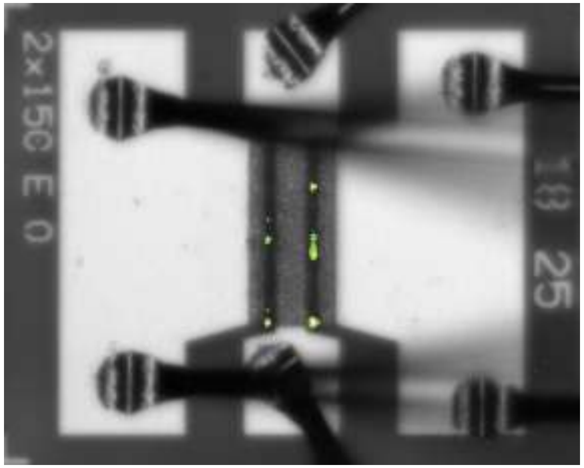




Forward Bias



Reverse Bias



Conclusion

- Off-state stress results in increase of non-radiative trap formation
- Negative temperature dependence with V_{CRI}, E_A= 38 meV.
- Exhibited similar gate leakage current before and after V_{CRI}, independent of critical voltage and stress temperature.

$\longrightarrow$ Current driven degradation mechanism

- Gate and drain lag decreases as stress temperature increased, indicating trap formation changes with stress temperature.
- RF stress shows threshold drain bias. Similar to V_{CRI}.
- Schottky contact likely reason for degradation
- E_A = 0.45 eV